IN THE CLAIMS:
Please revise the claims to read as follows:

1. (Currently Amended) An input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring, said protection device comprising:

a first region of a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the first diffusion layer having a second conduction type opposite the first conduction type ~~and~~, said first region being connected to the input/output terminal;

a second region of said first diffusion layer of the second conduction type being held at a predetermined potential; and

a third region having a diffusion layer of the second conduction type fabricated at a bottom of the second ~~diffusion layer~~ region, the third ~~diffusion layer~~ region being connected to the second region of first diffusion layer, said third ~~diffusion layer~~ region being fabricated at a location other than at a bottom of said first diffusion layer of said first region,

the first ~~diffusion layer~~ region being circularly enclosed ~~with~~ by the second and third ~~diffusion layer~~ regions, said first region, said second region, and said third region thereby forming a parasitic bipolar transistor in which said first region serves as a collector thereof and said second region and said third region serve as an emitter thereof.

2. (Original Claim) An input/output protection device in accordance with claim 1, wherein the region of the first conduction type of the semiconductor substrate includes a fourth diffusion layer having an impurity concentration higher than that of the semiconductor

substrate.

3. (Original Claim) An input/output protection device in accordance with claim 2, wherein the impurity concentration of the fourth diffusion layer monotonously decreases in a direction from a surface of the semiconductor substrate to an inner section thereof.

4. (Original Claim) An input/output protection device in accordance with claim 2, wherein the third diffusion layer has a depth equal to or more than that of the fourth diffusion layer.

5. (Original Claim) An input/output protection device in accordance with claim 1, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

6. (Original Claim) An input/output protection device in accordance with claim 1, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

7. (Original Claim) An input/output protection device in accordance with claim 1, wherein the first and second diffusion layers are manufactured with a gate electrode disposed on a surface of the semiconductor substrate.

8. (Original Claim) An input/output protection device in accordance with claim 6, wherein the device separating isolation layer or the gate electrode is fabricated in a circular shape.

9. (Original Claim) An input/output protection device in accordance with claim 7, wherein the gate electrode is connected to the signal wiring of the internal circuit of the semiconductor integrated circuit.

10. (Original Claim) An input/output protection device in accordance with claim 7, wherein the gate electrode is fixed to a predetermined potential.

11. (Original Claim) An input/output protection device in accordance with claim 1, wherein: the first conduction type is a p type and the second conduction type is an n type; and the predetermined potential is a ground potential.

12. (Original Claim) An input/output protection device in accordance with claims 1, wherein: the first conduction type is an n type and the second conduction type is a p type; and the predetermined potential is a potential of a power source.

13. (Previously Added) An input/output protection device in accordance with claim 3 wherein the third diffusion layer has a depth equal to or more than that of the fourth diffusion layer.

14. (Previously Added) An input/output protection device in accordance with claim 2, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

15. (Previously Added) An input/output protection device in accordance with claim 3, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

16. (Previously Added) An input/output protection device in accordance with claim 4, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

17. (Previously Added) An input/output protection device in accordance with claim 2, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a suffice of the semiconductor substrate.

18. (Previously Added) An input/output protection device in accordance with claim 3, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

19. (Previously Added) An input/output protection device in accordance with claim 4,

wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

20. (Previously Added) An input/output protection device in accordance with claim 5, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

21. (Currently Amended) An input/output protection device for a semiconductor integrated circuit, said protection device comprising:

a substrate having a first conduction type;

a first region having a second conduction type opposite said first conduction type, said first region connected to an input/output terminal;

a second region enclosing said first region, said second region having said second conduction type, said first region and said second region being electrically separated;

a third region formed adjacent said second region, said third region having said second conduction type, said third region being formed below said second region at a location other than at a bottom of said first region; and

a fourth region surrounded by said substrate and said first, second, and third regions, said fourth region having said first conduction type.

22. (Previously Added) The protection device of claim 21, where an impurity concentration of said fourth region decreases in a direction away from said first region.

23. (Previously Added) The protection device of claim 21, wherein said second region is connected to a first constant electrical potential.

24. (Previously Added) The protection device of claim 21, further comprising a MOS gate

structure for providing electrical separation between said first and second regions, said MOS gate structure including a gate electrode connected to a second constant electrical potential.

25. (Previously Added) The protection device of claim 23, further comprising a fifth region electrically isolated from said third region, said fifth region having said first conduction type, said fifth region connected to said first constant electrical potential.

26. (Previously Added) An integrated circuit having an input/output protection device of claim 21.

27. (Previously Added) The protection device of claim 1, wherein a protection of said internal circuit occurs by an avalanche breakdown in which said first diffusion layer connected to said input/output terminal serves as a collector and said second and third diffusion layers serve as an emitter for a lateral bipolar transistor.